BEE 271 Digital circuits and systems
Spring 2017 Syllabus

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Office hours TBD and by appointment
(I do not have an on-campus office.)

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Lectures Mondays and Wednesdays, 5:45 pm to 7:45 pm
Beardslee 260

Lab Mondays, 3:30 to 5:30 pm
Beardslee 220

Organization

BEE 271 introduces the basics of digital circuit and system design using Verilog, a hardware description language (HDL). We will cover the following topics:

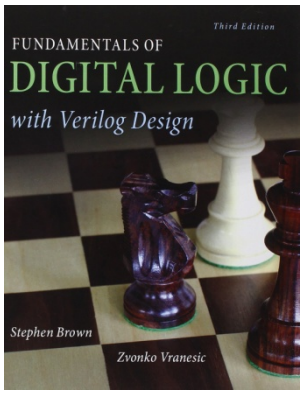
1. **Combinatorial logic.** Digital logic gates, Boolean algebra and logic minimization. These are non-clocked circuits like multiplexers and decoders whose outputs instantly reflect their inputs in ideal devices but which, in real devices, have propagation and rise and fall times.

2. **Synchronous sequential logic and finite state machines (FSMs).** These are clocked circuits that use flip-flops or registers and counters to capture state information. The next desired state is calculated using combinatorial logic based on the current state and any input and then copied into the state registers at the next clock.

3. **Verilog and FPGAs.** Verilog is a somewhat C-like programming language for hardware that allows us to describe the arrangement of combinatorial and sequential logic as if it was software. On a complex design, e.g., of an entire processor, Verilog is a lot easier to read and write than a huge schematic. We'll use it in the lab to program a field programmable gate array (an FPGA), a very cool device that can implement whatever logic we want.

Required text

We will be using this required text. I really like this book. It should be in the bookstore or easily available from Amazon and other sources. We'll cover the material in chapters 1 through 6 plus section 9.2 on hazards. You will also need to read Appendix A.



Fundamentals of Digital Logic with Verilog Design, Third Edition
Stephen Brown
Zvonko Vranesi
McGraw-Hill Education, 2013
ISBN 978-0073380544

Grading

Here's the weighting I will apply.

Homework	10%
Labs	30%
Midterm	30%
Final	30%

I grade on the curve, scaling the results so that most students will fall between 2.7 and 4.0 with median around 3.3. I deliberately weight homework very low as I intend for this to be practice that not everyone will need or have time to complete. Most students finish all the labs and do well on them, so most of the difference between a 2.7 and a 4.0 is determined by the exams.

Labs

There will be four labs.

1. Measuring the characteristics of physical logic devices.
2. A hex adding machine built using combinatorial logic in Verilog.
3. A keypad scanner using sequential logic.
4. A keypad debouncer.

You will be working in teams of two in the lab. It is up to you to choose a partner. For more on the labs, please refer to the lab rubric.

Homework

There will be six homework assignments at one to two-week intervals. You may work in pairs, same as you do on your labs.

Late policy

I am forgiving of late submissions in the lab, as described in the lab rubric, but not in the lecture portion of the course. Late homework will not be accepted.

All the work must be your own

You may certainly compare notes with other students and other teams and of course I understand that you may do research using Google. But absolutely everything you turn in to me must be your own work.

Neither I nor anyone else will proctor your exams in this course. It is my experience that people either rise to your expectations or not at all. I will, however, ask you to copy the following statement on your exams in your own handwriting and to sign your name to it.

> *On my honor, I will neither accept nor give unauthorized aid on this exam.*

If you misrepresent someone else's work as your own or if you try to deceive me in any of the myriad other ways that might seem attractive, and I discover it, you will get a zero on the assignment and I will report you for academic dishonesty. The one thing I've learned is that when you find someone has lied to you, all you really know for sure about them is that this isn't the first time. I do not give second chances. I report everything.

Disability

Access and Accommodations: Your experience in this class is important to me and to the University of Washington Bothell, where it is our policy and practice to create inclusive and accessible learning environments consistent with federal and state law.

If you experience barriers based on a temporary or permanent disability (including, but not limited to mental health, attention-related, learning, vision, hearing, physical or health impacts), please seek a meeting with Disability Resources for Students (DRS). They'll work with you and me and your other instructors to figure out some reasonable accommodations. The contact person is Rosa Lundborg at 425-352-5307 or email rlundborg@uwb.edu.

If you have already established accommodations with DRS, please tell me what they are so I can be sure to provide them.